

Claims

What is claimed is:

- 1 1. A method for implementing customized silicon wafer chip carrier passive devices comprising the steps of:
 - 3 receiving system design inputs for a package arrangement;
 - 4 generating a respective physical design for customized passive devices, a logic chip, and a chip carrier;
 - 6 fabricating silicon devices utilizing the generated respective physical design for customized passive devices and the logic chip;
 - 7 fabricating a carrier package; and
 - 8 assembling the fabricated silicon devices on the carrier package.
- 1 2. A method as recited in claim 1 wherein the step of assembling the fabricated silicon devices on the carrier package includes the steps of mounting silicon capacitors directly onto the carrier package.
- 1 3. A method as recited in claim 1 wherein the step of assembling the fabricated silicon devices on the carrier package includes the steps of mounting silicon resistors directly onto the carrier package.
- 1 4. A method as recited in claim 1 wherein the step of assembling the fabricated silicon devices on the carrier package includes the steps of using flip-chip mounting methods for assembling silicon chips onto the carrier package.
- 1 5. A method as recited in claim 1 wherein the step of generating a respective physical design for customized passive devices, a logic chip, and a chip carrier includes the steps of generating a physical design for a silicon capacitor chip having a selected capacitor shape.
- 1 6. A method as recited in claim 1 wherein the step of generating a respective physical design for customized passive devices, a logic chip, and a chip carrier includes the steps of generating a physical design for a silicon capacitor chip having a selected capacitor size.

1 7. A method as recited in claim 1 wherein the step of generating a
2 respective physical design for customized passive devices, a logic chip, and
3 a chip carrier includes the steps of generating a physical design for a silicon
4 capacitor chip having a selected number of capacitor connections.

1 8. A method as recited in claim 1 wherein the step of receiving
2 system design inputs for a package arrangement includes the steps of
3 receiving voltage and current limits.

1 9. A method as recited in claim 1 wherein the step of receiving
2 system design inputs for a package arrangement includes the steps of
3 receiving system targets and a frequency specification.

1 10. A method as recited in claim 1 wherein the step of receiving
2 system design inputs for a package arrangement includes the steps of
3 receiving logic chip parameters.

1 11. A method as recited in claim 1 wherein the step of receiving
2 system design inputs for a package arrangement includes the steps of
3 receiving chip carrier package specifications.

1 12. A method as recited in claim 1 wherein the step of receiving
2 system design inputs for a package arrangement includes the steps of
3 receiving cost target specifications.

1 13. A method as recited in claim 1 wherein the step of fabricating
2 silicon devices utilizing the generated respective physical design for
3 customized passive devices and the logic chip includes the steps of defining
4 silicon chip decoupling capacitors and silicon resistors from selected areas
5 of a silicon wafer used for forming the logic chip.

1 14. A method as recited in claim 1 wherein the step of fabricating
2 silicon devices includes the steps of dicing silicon chip decoupling capacitors
3 from a peripheral area of a silicon wafer.

1 15. Apparatus for implementing customized silicon wafer chip
2 carrier passive devices on a carrier package arrangement comprising:
3 a silicon passive devices customizing program for receiving system
4 design inputs for a carrier package arrangement;
5 said silicon passive devices customizing program for generating a
6 respective physical design for customized passive devices, a logic chip, and
7 a chip carrier; for fabricating silicon devices utilizing the generated respective
8 physical design for customized passive devices and the logic chip and for
9 fabricating a carrier package; and
10 said silicon passive devices customizing program for assembling the
11 fabricated silicon devices onto the carrier package.

1 16. Apparatus for implementing customized silicon wafer chip
2 carrier passive devices as recited in claim 15 wherein the system design
3 inputs include at least one of voltage and current limits; system targets and a
4 frequency specification; logic chip parameters; chip carrier package
5 specifications; and cost target specifications.

1 17. Apparatus for implementing customized silicon wafer chip
2 carrier passive devices as recited in claim 15 wherein said silicon passive
3 devices customizing program for assembling the fabricated silicon devices
4 onto the carrier package includes said silicon passive devices customizing
5 program for assembling the fabricated silicon capacitors directly onto the
6 carrier package.

1 18. Apparatus for implementing customized silicon wafer chip
2 carrier passive devices as recited in claim 15 wherein said silicon passive
3 devices customizing program for generating a respective physical design for
4 customized passive devices includes said silicon passive devices
5 customizing program for generating a physical design for a silicon capacitor
6 chip having a selected capacitor shape; a selected capacitor size; and a
7 selected number of capacitor connectors.